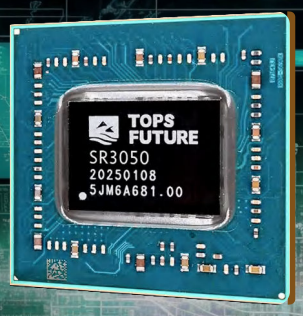
SR3050



The SR3050 is a general computing platform for industrial controllers, raspberry computers, micro routers. It enables people of all ages to explore computing, to learn how to program in languages like Scratch and Python, to easily develop digital maker projects(e.g. music machines, parent detectors, weather stations, tweeting birdhouses with infra-red cameras).

Key Features

Core Processor

- Quad-core 64-bit RISC-V CPU(RV64GCV, C920), up to 2.0GHz
- Support RISC-V Vector for FP16/ FP32/ FP64
- FPU integrated
- 64KB L1 Instruction Cache and 64KB L1 data cache, 1MB L2 cache
- DVFS supported

SAP

- Secure Assistant Processor
- T-HEAD E906, up-to 500MHz
- 32-bit processor, RISC-V compatible
- RV32IMC Instruction set

Display

- QSPI interface 1/4 wires
- QSPI interface up to 100MHz

Peripheral Interface

- 6 I2C Interface/ 4 UART/ 4 SPI/ 2 I2S/ 8 PWM
- 99 GPIO With Interrupt Capability
- 4 USB/ 2 Ethernet

System Peripherals

- 16 Channel DMA
- Watchdog Timer
- RTC (Real Time Clock)
- PLL/ PVT/ Mailbox(MU)

Memory

1 DDR Memory Port

- LPDDR4/LPDDR4X interface
- 32-bit bus width
- up to 2133MHz

External memory

- xSPI Nor/Nand Flash, up to 4 or 8 wire
- eMMC
- SDHC

CAE

- Dual Cryptography Accelerator Integrated
- Support Up To 750MHz For Single Core
- IPsec/ SSL/ TLS/ DTLS 3.1Gbps Using AES And SHA-1 For Single Core
- MACsec 3.7Gbps Using AES-GCM For Single Core

Physical

- Power Supply
  - Core: 0.8V
  - IO: 1.8V/ 3.3V
  - Analog 1.1V(LPDDR4)/ 0.6V(LPDDR4X)/ 1.8V(PVT)
- Temperature: -30°C ~ 85°C
- Typical Power Consumption: 5W
- Package: FCBGA, 784pin, 19mmx19mm

Block Diagram